In the Abstract of the Disclosure:

~~To provide a~~ A phase detector circuit that prevents a significant loss of lock during input of CIDs (Consecutive Identical Digits) and ~~have~~ has a high linearity of a phase to voltage conversion characteristic around a phase-locked point in an operation of comparing phases of random NRZ signals in a phase. By using the phase detector circuit having a circuit configuration ~~represented by a formula (1) or (2), for example, a circuit configuration shown in FIG. 11~~ containing a delay circuit and a combination of least a multiplier circuit and a subtractor circuit, a capability as the PLL circuit of preventing the significant loss of lock can be realized. In addition, since a duty cycle of a pulse appearing at an output terminal 3 of a multiplier circuit 62 approaches 50% as a phase-locked state is approached, a distortion in the phase to voltage conversion characteristic does not appear, and ~~the~~ thus high linearity of the phase to voltage conversion characteristic around a phase-locked point can be realized.